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IMPLEMENTATION OF LOW COMPLEX UNIVERSAL FILTERED MULTICARRIER

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ABSTRACT

In 5G technology for enhancing the high speed data process the Filter Bank Multicarrier (FBMC), Universal Filtered multicarrier (UFMC), and Generalized Frequency Division Multiplexing (GFDM) techniques are used in effective manner. The FIR filter plays an important role in 5G mobile communication technology. In this paper, the hardware complexity reduced by using the FIR filter. In previous technique, 73 multipliers are required to the filtering process. Here to reduce the number of multipliers by using the multiplexers. The 73 multipliers to be replaced with the 5 number of 16:1 multiplexers, 5 multipliers and 4 registers. The Multiple Constant Multiplication (MCM) scheme is also presented for the block implementation FIR filters. Reducing the memory usage for using the less number of multipliers. Use the less number multipliers the difficulties are to be reduced. The overall implementation has a result of 42% reduction in hardware complexity.

INTRODUCTION

In the design of the circuit to be mainly considered the power, area, delays. These are the important parameter for the wireless system network. The usage of area and delay is minimum considered as the important challenges. The main aim is to be reducing the power consumption in recently. The devices integration level is to be increased and it will also growth the complexity of micro-electronic circuit.

Cyclic Prefeix – Orthoganal Frequency Division Multiplexing (CP-OFDM) has the better spectral properties. It contains many multicarrier systems. The all multicarrier systems has more advantages. The size of the each packets are flexibility and it has more spectral bandwidth, Peak to Average Power Ratio (PAPR). These are the important characteristics for which the waveform can be evaluated[2].

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The long sequence data transmission and very short packet transmission process to be used the UFMC. It is better than FBMC[3]. The transformation of filtering operation into FFT as special cases along with the cyclic prefix, fast-convolution implementation of the Multicarrier filter bank based waveform is implemented and analyzed[4].

The operation of UFMC is simpler than operation of FBMC. It is easy to convert the CP-OFDM to UFMC. GFDM is used to the pulse shaping method for avoid and it will be reduce the Inter Carrier Interference (ICI) and cyclic prefixes. These are used to compensate the Inter Symbol Interference (ISI). The all multicarrier systems is used to the linear convolution method it will be given the lower symbol length compared to FBMC [5]. The OFDM produce the high out-of-band radiations.

The main drawback of the OFDM it is very sensitivity during the Carrier Frequency Offset (CFO) and Timing Offsets (TO). It provides more side lobe for data processing[6].

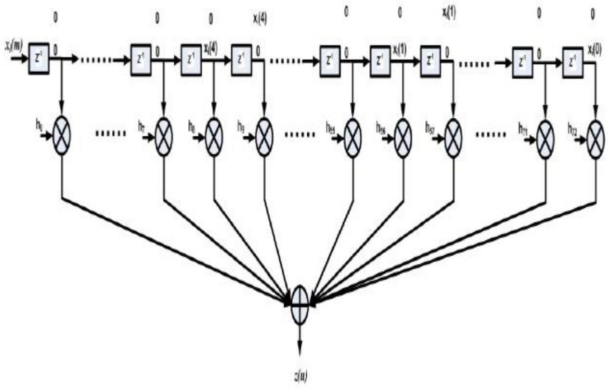
Here resource blocks (RB) split into two subgroups. These subgroups are named odd and even. Then filtering operation is to be applied the each subgroups.it will be reduced the number of Inverse Fourier Transform (IFT) and filtering convolutions. The increasing the number of subcarriers level to take more processing time. The result indicates the output of the OFDM system it is same operation of the UFMC system[11].

In this paper Generalized Synchronous (GS) Multi-Services (MS) Sub Band Filtered Multicarrier (SFMC) technique to be used and equalization algorithm is proposed. Here the overcome the all above drawbacks and to reduce the hardware complexity and it achieved the scalability and flexibility requirement. It is also used to high processing data speed requirement. Using the different filter coefficient achieved the flexibilty.it is used the separate memory space.

EXISTING MODEL

In this method to be used the 73 tap FIR filter. Here the each input coefficient required the separate multiplier and register to be stored. The first input x (1) is multiplied with the h72, next input is x (2) multiplied with the h56 and so on. The samples are shifted by using the next filter output coefficient in right one positioning. The figure1 showed the architecture of existing technique.

Figure – 1: *Existing FIR Filter Design Model*



After the IDFT operation using 15 zeroes to get the up sampling factor. Each coefficient is multiplied with the separate input x (n) and it multiplied continuously. Finally, all the multiplied values are added and get the output y (n). Here the each

coefficient to require the separate multiplier and adder. The figure 1 showed the architecture.

REDUCED COMPLEXITY FIR FILTER

The drawback of existing method is to be overcome here. In this proposed method to be reducing the number of multipliers by using the non-zero samples. The non-zero samples are multiplied with the filter coefficient. The 73 multipliers by replacing of the 5 16:1 multiplexers, 4 shift register, and 4 adders. Here the zero padding cannot be performed.

The first input x (m) enters the filter, it is to be stored memory element and it to be shifted, the next 16 cycle of the filter coefficient. The multiplier multiplied the output of the multiplexer and given input value x (m). In this process to performed the each next 16 cycle of filter coefficients. Finally, the multiplied value is to be added. The number of multipliers can be reduced by using the non-zero samples and filters coefficients. Multiplication of these two elements to be reduced the number of multipliers.

Figure – 2: *Proposed FIR System Model*

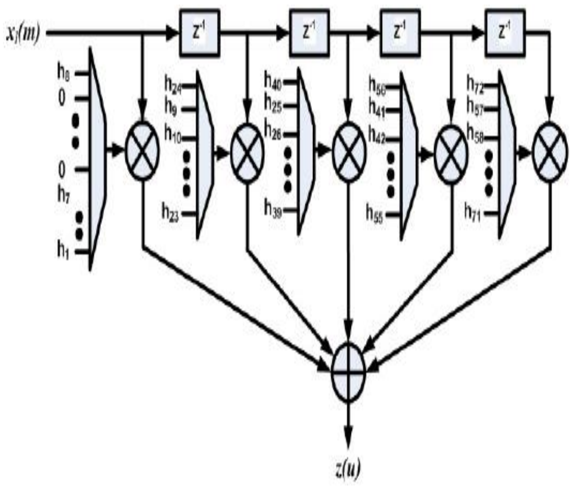
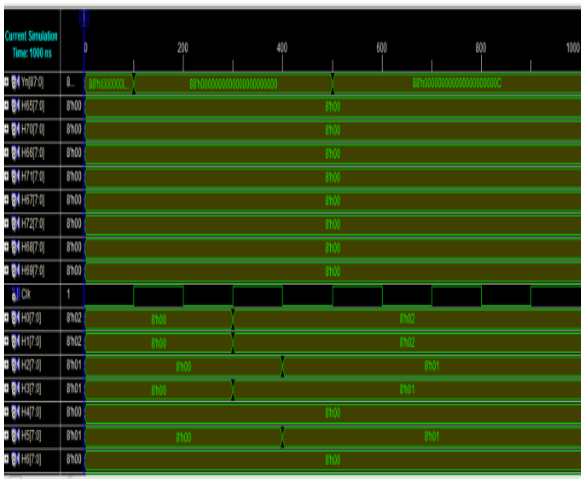


Figure – 3: *Output for 73 Tap FIR Filter*



Here to use 16:1 multiplexers to be used. It required the 16 input and 4 select lines. Multiplexers are used to measure the input quantity size, bandwidth time. A multiplexer is additionally called as an information selector. It is likewise used to execute the Boolean capacity of numerous factors. The operation is to be performed by order of the coefficients.

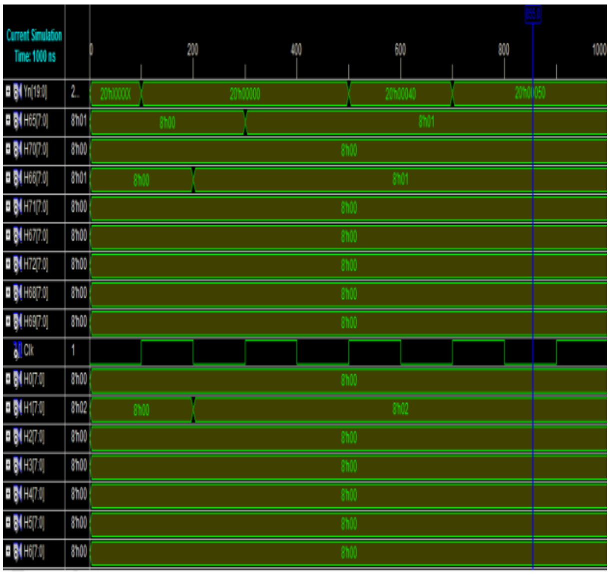
SIMULATION RESULTS

In this section the simulation result of 73 tap FIR filter which may uses larger number of multipliers in it and having more delay element in it. Such result can be shown in the Figure 3.

The proposed work model by using multiplxer has been implemented in xilinx software and such output obtained for the newly proposd FIR filter will be illustrated in the figure 4.

In such output the complexity is much more reduced when compared to the 73 tap FIR filter. And number of multipliers used will also be reduced in this proposed model.

Figure – 4: *Output for Proposed Method*



COMPARISON OF FIR FILTER RESULT

Sl. No.	73 Tap FIR Filter	FIR Filter using Multiplexer
1.	73 multiplier and 73 delay elements are to be used	5 multipliers and 4 delay elements are to be used.
2.	Inputs is given to a separately.	Here the input is given in to 16 cycles.
3.	To perform the IDFT operation it required the zero padding.	It is not require the zero padding.
4.	The total memory usages are 375652 kilobytes.	The total memory usages are 171556 kilobytes.

CONCLUSION

If there is an occurrence of single and multiple services then UFMC is employed since it generates the required waveform. In filtering section is proposed which can be avoided the number of multiplications processes involved in the FIR filter. Subsequently, the 5 multipliers, 5 multiplexers and 1 adders is required instead of 73 multipliers, shift registers and adders. In this FIR filter design to occupy the less number of memory space and it processing speed is to be high. This FIR FILTERS are to be used for the complex multiplication applications and it suitable for UFMC waveform generation.

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